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Ultra-High Cell Density TrenchFET® Devices: Obtaining the Critical Balance of Switching Performance Versus On-Resistance and Its Associated Impact on Device Selection

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Abstract

With the recent introduction of MOSFET cell densities in excess of 100M cells per square inch, the power electronics designer now has available a significant weapon in the ever-increasing battle to raise overall dc-to-dc converter efficiency. However, groundbreaking advances in certain device performance parameters come at a cost to others, so this new technology must be scrutinized, analyzed, and understood.

The ultra-high density process is a breakthrough; however, without a thorough understanding of the results and their consequences, the technology easily could become limited in its field of usage. Discussion will be given to the main vertical scaling and its effects on device on-state parameters versus the compromise to gate input capacitance and charge. Details will be given to show how a combination of not only vertical but also lateral scaling of the device gate-trench structure can help address balance and offer the choice of both low-level on-resistance and gate charge.

Actual results will be used to compare and contrast different cell density devices, ranging from 32M up to >100M cells per square inch, in relation to all main performance criteria. Graphical examples will be shown and results discussed of converter topology efficiencies using different cell density MOSFETs under differing switching and load conditions.

1.0 TrenchFET® Ultra-High Cell Density

With the edict from dc-to-dc circuit manufacturers to design high-density converters with improved efficiency, smaller footprints, and lower cost despite increasing output loads, there is a huge consequent pressure on power MOSFET suppliers to produce better-performing devices. Generally speaking, driving factors are low $r_{DS(on)}$; higher efficiency; lower power dissipation and subsequently a smaller or no heatsink; improved reliability; improved UIS; lower component count – eliminating the need to parallel; lower gate charge and capacitance; faster switching speeds and reduced switching losses; increased power package density; and finally, reduced manufacturing costs. This is no small task.

Two common dc-to-dc circuit topologies that utilize the MOSFET as a switching device are the synchronous buck converter, as commonly found in portable computer power management systems, and the secondary rectification MOS pair as seen in dc-to-dc converter synchronous outputs. For the purposes of evaluation and comparison, these two circuits only will be the focus of this paper.

The following sections will highlight the strengths gained and balance achieved when designing with new TrenchFET ultra-high density silicon MOSFETs in relation to the desired dc-to-dc application, as well as identify important considerations and selection criteria to be addressed.

1.1 Increasing the Cell Density

Trench-gated vertical DMOS silicon is commonplace in today's industry, providing well-known, documented, and established advantages over its planar counterparts.

MOSFET silicon innovation with Vishay Siliconix is ongoing with TrenchFET Generation 1 being the baseline for the industry's Trench technology. Generation 2 has a shallow source, lower V_{th}, and a thinner substrate – hence providing improvements in $r_{DS(on)}$.

Typical Generation 2 densities for n-channel and p-channel trench devices alike range between 32M to 50M cells per square inch. Both the static and dynamic performance of 32M cell trench devices is impressive. Depending on specific manufacturing processes, on-resistances of the industry's better SO-8 30-V n-channel devices (the dc-to-dc benchmark) are in the 4-mΩ to 5-mΩ region with gate charge levels (Q_g) of <25 nC in the Si4842DY, for example.

To increase cell density, device engineers have to focus primarily on lateral scaling of the cells. With lateral scaling, the density per wafer obviously will increase dramatically, thereby lowering the overall on-resistance. However, for high switching dc-to-dc applications, the ultra-low $r_{DS(on)}$ is only half the focus, as P_d totals combine conduction, gate, and switching performance.

To achieve optimum MOSFET silicon performance, both lateral and vertical scaling have to be implemented. By using in-house fab facilities, Vishay Siliconix is able to lateral scale cell density to more than 170M cells per square inch, and to vertical scale the trench to minimize the gate capacitance and keep total gate charge (Q_g) to levels previously seen only in lower cell density devices (sub 40 nC). Figure 1 shows the difference between existing 32M cell density and the effects of improving, both laterally and vertically, the cell structure on the latest higher-density generation silicon.

From the two cell cross-sections, it can be seen that MOSFET lateral scaling results in fine patterning, scaling of channel width, smaller die area, and consequently lower $r_{DS(on)}$. The vertical scaling improvement gives a low thermal budget, thin epi-layer, short channel, and shallow trench, resulting in Q_g minimization.

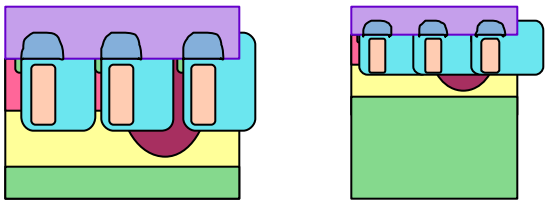

Figure 1. Comparison of vertical and lateral technology improvements against existing silicon structures

Vishay Siliconix's Generation 3 silicon technology development combines both vertical and lateral scaling methods to shorten the channel, lowering the $r_{DS(on)}$, and to implement a shallow junction and shallow trench process that reduces C_{gs} and C_{gd} to provide low $r_{DS(on)} \times Q_g$ for higher-frequency PWM optimization.

Figure 2 shows the effect of shallower trench depth on FET gate turn-on characteristics. The Miller capacitance and consequent plateau on the V_{gs} turn-on is effectively reduced, hence the device will be fully saturated faster than longer-trench-depth silicon.

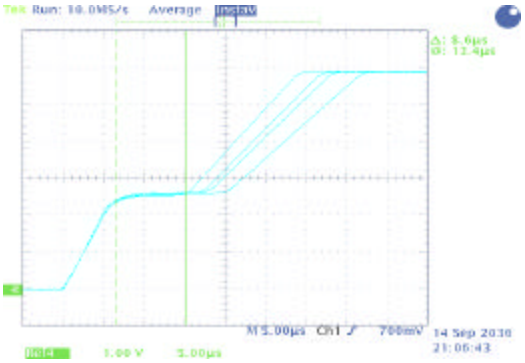

Figure 2. Shallow-trench-depth reducing the Miller effect

On paper it is clear to the designer that TrenchFET silicon advances offer significant characteristic improvements, both static and dynamic, over today's industry-leading devices. However, no device, even new-

generation silicon, can offer the best parameters in all performance areas. This is where the manufacturer will optimize according to the design, and the designer will optimize depending on the circuit.

2.0 MOSFET Device Optimization for Synchronous DC-to-DC Applications

It is no longer acceptable to compromise dc-to-dc converter efficiency by selecting an established, standard device. Take the 30-V n-channel Si4420DY SO-8 MOSFET, for example. As the Generation 1 device of choice for dc-to-dc synchronous buck or secondary rectification converters just two years ago, it was an industry leader. The Si4420DY has a maximum on-resistance value of 9 mΩ at a 10-V V_{gs} and typical gate charge of 35 nC, which still can be classed as a low figure of merit of 315.

A comparison of this device against a Generation 2 technology device, the Si4880DY, immediately demonstrates an improvement laterally, with lower $r_{DS(on)}$, and more important, a reduction in total gate charge (Q_g) to 19.5 nC – hence an overall FOM of 158. The Si4880DY has a maximum on-resistance of 8 mΩ at a 10-V V_{gs} and typical gate charge value of 19.5 nC. Effectively, this is a 50% reduction from the Si4420DY. Lower $r_{DS(on)}$ means lower conduction losses and lower Q_g, resulting in lower switching losses. Figure 3 compares the Si4420DY against the Si4880DY in a like-for-like efficiency evaluation.

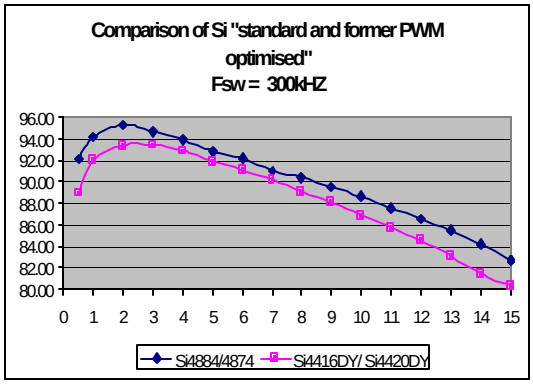

Figure 3. Synchronous buck efficiency comparisons

Each device was used in both the high-side and low-side, driven by the same synchronous buck controller at 300 kHz. A 1% increase in controller efficiency was gained by simply substituting the Si4880DY for the Si4420DY.

Now with the ability of both vertical and lateral scaling in the latest silicon technology process, the best balance of $r_{DS(on)}$ and Q_g can be obtained – and produced according to respective circuit requirements. Reducing C_{gs} and C_{gd} will lower the overall Q_g to record-low levels, and shorter channels will offer SO-8 n-channel 30-V MOSFETs with $r_{DS(on)}$ values below 4.5 mΩ. The Si4364DY, for example, has a maximum $r_{DS(on)}$ at 10 V of 4.25 mΩ.

2.1 High-Side and Low-Side Selection

A synchronous rectification converter secondary contains two MOSFET switches, the high side (or inline switch) and the low side (or flywheel switch). Due to the circuit operation, it is known that each switch, high-side or low-side, requires differing criteria to achieve optimum converter efficiency. Traditionally, the standard design approach was to use the same low-$r_{DS(on)}$ and low-Q_g device in both high-side and low-side slots. This is adequate, and with low FOM devices, reasonable efficiencies can be achieved.

Today, however, further improvements can be achieved by optimizing respective device selection with the new array of latest-generation devices available. So when the cost-per-amp or size-per-amp of generic dc-to-dc converters must be reduced, then switching frequencies have to increase, passive component size must be reduced, and the overall efficiency has to increase, which means that even a 1% increase is significant.

High-side switch selection is the simpler choice, as it will be affected by both switching and conduction loss. Therefore, the lowest FOM is desirable.

When examined in more detail, the ideal high-side switch must have:

a.) Small R_g and L_s to cut the time constants ($T_c = R_g(C_{gs} + C_{gd1})$), small C_{iss} for short current transients, and small C_{gd} for short voltage transients – all to reduce the overall switching loss;

b.) Small Q_g (and hence C_{iss} and C_{gd}) to reduce the gate charge losses; and

c). Lowest $r_{DS(on)}$ to reduce the conduction losses.

So, in relation to silicon technology (G3 process) the device requires shallow trench and short channel length for optimum FOM.

Looking at the low side, there are far more direct and indirect operational parameters and requirements. In summary:

Event	Issue	Parameter
Turn-off	**Ringing**	$T_f - R_g C_{iss}/V_{th}$
Turn-on	**Body diode**	$T_r - R_g C_{iss}/(V_{gs}-V_{th})$
Conduction	**Low $r_{DS(on)}$**	$r_{DS(on)} - 1/(V_{gs}-V_{th})$

The low side device requires:

a.) Ultra-low $r_{DS(on)}$ to reduce conduction losses;

b.) Small Q_g (hence C_{iss} and C_{gd}) to reduce the gate charge loss; and

c.) Q_{gd}-to-Q_{gs} ratio of <1.0 to enable the device to be shoot-through-rugged.

For synchronous rectification the switching losses of the low-side device are not applicable, as the parallel body drain diode or externally connected Schottky diode is in conduction immediately prior to current transferring to the FET. As a result, there is no voltage V_{ds} to decay across the MOSFET.

Therefore, in relation to silicon technology (G3 process), the low-side device requires high density and short channel length for lowest resistance and small Q_{gd} to avoid shoot-through conditions. The further benefit of complete silicon manipulation for third-generation technology is the ability to make dc-to-dc switching devices (low-side) shoot-through-rugged. The Q_{gd} / Q_{gs} is <1.0 and thus there are no issues at switching both devices at speeds in excess of 300 kHz.

Traditionally with non-PWM-optimized devices, increasing the switching speed naturally gave rise to greater dv/dt and di/dt switching overshoots. A common problem was that the higher switching transition of the high-side device caused spurious charging of the C_{gd} of the low-side switch and hence a consequent transient voltage on the low-side gate and, finally, turn-on and shoot-through from dc rail to ground. Therefore, the aim of raising the switching frequency to reduce the size of circuit passive components was counterproductive unless the selection of device (especially the low side) could be manipulated to resist any occurrence of spurious turn-on. Approximate calculation and practice show the order of Q_{gs} to equal two times the Q_{gd} for shoot-through-rugged devices.

3.0 Results of High-Side and Low-Side Device Selection

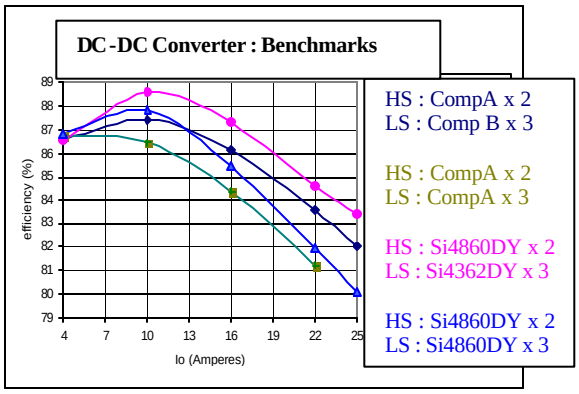

Figure 4: DC-to-DC device benchmarking

Figure 4 above shows an important comparison of differing high-side and low-side device optimization. Each test was performed using the same synchronous buck converter, load, and circuit with the devices (two in parallel for the high-side and three in parallel for the low-side) switching at a constant 300 kHz and 20-V input with a 1.5-V output.

From the four device selections shown, it is possible to compare the traditional approach of using the same 30-V n-channel SO-8 FET

as both high-side and low-side. The least-efficient result used the competitor's device A, selected as the best-from-family for low $r_{DS(on)}$ and low Q_g (FOM = 216). The data is shown in green [squares ¦] and, under light loading, gives only 86.8% efficiency at best.

The data line in light blue [triangles ?] uses the Si4860DY, a Generation 2 technology device from Vishay Siliconix (8 mΩ and 13 nC, FOM = 104) as both high-side and low-side. The result gives an impressive 88% efficiency at light loads but falls steadily under increased current.

The data shown in dark blue [diamond ?] uses competitor A devices on the high-side (both low $r_{DS(on)}$ and low Q_g) and competition B devices on the low-side (best-in-family $r_{DS(on)}$ and consequently higher Q_g, FOM = 174). The efficiency is reasonable under light loads (87.5% maximum) but remains high as the load is increased.

Finally, and the ultimate point of the evaluation, there is the data curve shown in pink [circle ?]. This line uses Si4860DY devices in the high-side (low $r_{DS(on)}$ and low Q_g) and Si4362DY in the low-side. The Si4362DY is the first of the Vishay Siliconix Generation 3 technology n-channel products at 113M cells per square inch. This device has been optimized for ultra-low on-resistance and normal levels of Q_g (4.5 mΩ and 42 nC, FOM = 189). The effect of selecting such as a high-side and low-side optimized pair is to achieve a maximum efficiency of 88.8% under light load whilst still remaining >1% better than the nearest rival combination as the load increases.

4.0 Conclusions

The object of this paper was to inform the reader of the groundbreaking advances in MOSFET silicon technology in relation to devices selected for low-voltage, higher-frequency dc-to-dc power conversion. By making real circuit comparisons between Vishay Siliconix traditional, recent, and new silicon technologies, the designer can see and appreciate the subtle improvements, which often hide behind obvious data sheet parameters, in relation to increasing converter switching speeds.
Not only Q_g for lower switching losses but also the ratio of Q_{gs}/Q_{gd} have been highlighted as areas of manipulation to give shoot-through-rugged devices. The important physical silicon properties that affect gate and switching characteristics of the new PWM Generation 3 optimized TrenchFETS also have been demonstrated.

Discussion was also given to selection – through both traditional and new device parameters – from what is now a huge array of MOSFET secondary devices. More specifically, the designer can manipulate differences in high-side and low-side operations to meet the circuit demand and achieve greater efficiency by making the appropriate choice rather than choosing a standard approach.

The differences between the different technological generations plus manipulation of high-side or low-side choice was shown effectively in Figure 4, in that efficiency increases of >2% can be achieved by selection of low-FOM silicon for the high-side and only low-$r_{DS(on)}$ silicon for the low-side.